Application No. 10/595,658

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of:

Applicant: Adam CAPEWELL et al.

Application No: 10/595,658

Filing Date: May 3, 2006

Title: FORMATION OF LATTICE-TUNING SEMICONDUCTOR SUBSTRATES

REQUEST FOR CORRECTED FILING RECEIPT

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
10/595,658	10/07/2008	2812	1030	MARSP0175US	17	1

CONFIRMATION NO. 4245

43076
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FILING RECEIPT

OC000000032822796

Date Mailed: 10/29/2008

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Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP04/50022 10/28/2004

Foreign Applications

UNITED KINGDOM 0326321.7 11/12/2003

PCT/GB2004/050022

If Required, Foreign Filing License Granted: 10/27/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 10/595,658**

Projected Publication Date: 02/05/2009

Non-Publication Request: No

Early Publication Request: No

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 May 2005 (26.05.2005)

PCT

(10) International Publication Number
WO 2005/048330 A1

(51) International Patent Classification[7]: H01L 21/20, C30B 25/04

(21) International Application Number: PCT/GB2004/050022

(22) International Filing Date: 28 October 2004 (28.10.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0326321.7 12 November 2003 (12.11.2003) GB

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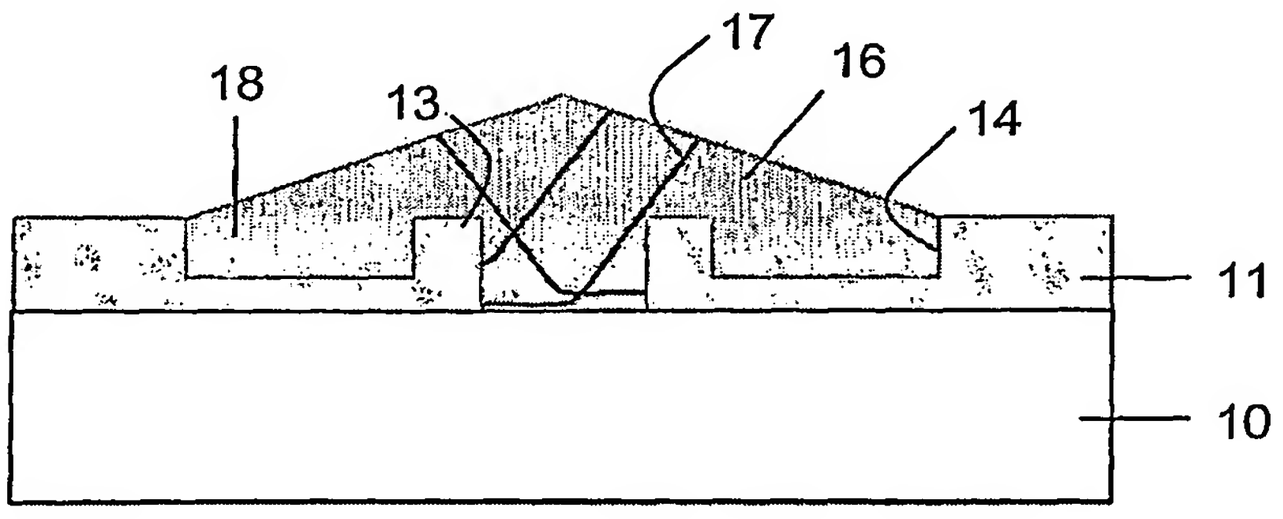
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *with amended claims and statement*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FORMATION OF LATTICE-TUNING SEMICONDUCTOR SUBSTRATES



(57) Abstract: A method of forming a lattice-tuning semiconductor substrate comprises defining a selected area (12) of a Si surface (15) by means of a window (13) extending through an isolating layer (11) on the Si surface (15); defining in the isolating layer (11) a depression (14) separated from the Si surface (15) by a portion of the isolating layer (11); growing a SiGe layer (16) on top of the selected area (12) of the Si surface (15) such that dislocations (17) are formed in the window (13) to relieve the strain in the SiGe layer (16); and further growing the SiGe layer (16) to overgrow the isolating layer (11) and extend into the depression (14) to form a substantially dislocation-free area (18) of SiGe within the depression (14). If required, the portion of the SiGe layer (16) that has overgrown the isolating layer (11) can then be removed by polishing so as to isolate the substantially dislocation-free area (18) of SiGe within the depression (14) from the area of SiGe within the window (13). Furthermore the SiGe layer (16) and the isolating layer (11) can then be removed from the Si surface (15) except in the vicinity of the depression (14) so as to leave on the Si surface (15) the substantially dislocation-free area (18) of SiGe isolated from the Si surface (15) by the portion of the isolating layer (11).

WO 2005/048330 A1